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10/699,668	11/04/2003	Kenji Kasahara	740756-2657	6475

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EXAMINER	
MAI, ANH D	

ART UNIT	PAPER NUMBER
2814	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/699,668	KASAHARA, KENJI	
	Examiner	Art Unit	
	Anh D. Mai	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 October 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/19/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Status of the Claims

1. Amendment filed October 19, 2005 has been entered. Claims 31-33 have been added. Claims 1-33 are pending.

Information Disclosure Statement

2. The information disclosure statement filed October 19, 2005 fails to comply with the provisions of 37 CFR 1.97, 1.98 and MPEP § 609 because the reference appears to be a definition of some form with hand written foot note on the side, thus it is not proper. It has been placed in the application file, but the information referred to therein has not been considered as to the merits. Applicant is advised that the date of any re-submission of any item of information contained in this information disclosure statement or the submission of any missing element(s) will be the date of submission for purposes of determining compliance with the requirements based on the time of filing the statement, including all certification requirements for statements under 37 CFR 1.97(e). See MPEP § 609.05(a).

Claim Objections

3. New claims 31-33 are objected to because of the following informalities:

All three claims recite: an impurity.

The correct term is "said" or "the" because *impurity* have been referred to in claims 1, 7 and 17, unless applicant means another kind of impurity which is differed than that of claim 1, 7 and 17.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-5, 7-11, 13-16, 31 and 32 are rejected under 35 U.S.C. 102(b) as being anticipated by Yamazaki et al. (EP. Patent No. 0485233) of record.

With respect to claim 1, Yamazaki teaches a semiconductor device as claimed including:

a substrate (11);

a first insulating film (32a) provided over the substrate (11);

a second insulating film (32b) provided over the first insulating film (32a);

a semiconductor film (33) provided over the second insulating film (32b);

a source region and a drain region (34) provided in the semiconductor film (33);

a channel region (28) provided in the semiconductor film (33) between the source region and drain region (34); and

a gate electrode (40) provided over the channel region (28) with a gate insulating film (35) therebetween,

wherein an impurity concentration in an interface between said first insulating film (32a) and the second insulating film (32b) is (E19-E21 atom-cm^{-3}) higher than an impurity

concentration in an interface between the second insulating film (32b) and the channel region (28) (E11 atom-cm^{-3}). (See Fig. 11A).

With respect to claim 7, Yamazaki teaches a semiconductor device substantially as claimed including:

a substrate (11);

a first insulating film (32a) provided over the substrate (11);

a second insulating film (32b) provided over the first insulating film (32a);

a semiconductor film (33) provided over the second insulating film (32b);

a channel region (28) provided in the semiconductor film (33); and

a gate electrode (40) provided over the channel region (28) with a gate insulating film (35) therebetween,

wherein an impurity concentration in an interface between said first insulating film (32a) and the second insulating film (32b) is (E19-E21 atom-cm^{-3}) higher than an impurity concentration in an interface between the second insulating film (32b) and the channel region (28) (E11 atom-cm^{-3}). (See Fig. 11A).

With respect to claims 2 and 8, semiconductor device of Yamazaki is capable of incorporated into one selected from the group consisting of a personal computer, a video camera, a mobile computer, a goggle type display, a player using a recording medium, a digital camera, a cellular phone, and an electronic book, as claimed.

With respect to claims 3 and 9, the semiconductor film (33) of Yamazaki comprises a material selected from the group consisting of silicon and Si_xGe_{1-x}.

With respect to claims 4 and 10, the semiconductor film (33) of Yamazaki comprises crystalline semiconductor.

With respect to claims 5 and 11, the substrate (11) of Yamazaki is selected from the group consisting of an insulating substrate.

With respect to claims 13 and 15, the second insulating film (32b) of Yamazaki comprises a material selected from the group consisting of silicon oxide.

With respect to claims 14 and 16, the first insulating film (32a) of Yamazaki comprises a material selected from the group consisting of silicon oxide.

With respect to claims 31 and 32, since the first insulating film was exposed to oxygen in the doping step, thus, the impurity of Yamazaki comprises oxygen.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 6 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki '233 as applied to claims 1 and 7 above, and further in view of Kim et al. (U.S. Patent No. 6,100,954) of record.

Yamazaki teaches the semiconductor device as described in claims 1 and 7 above including a gate insulating film (35) formed between the gate electrode (40) and the channel region (28).

Thus, Yamazaki is shown to teach all the features of the claim with the exception of utilizing organic resin for the gate insulating film.

However, Kim teaches a semiconductor device having a gate insulating film (157) comprising an organic resin (BCB) is formed between a gate electrode (113) and channel region (119). (See Fig. 13D).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the gate insulating film of Yamazaki utilizing organic resin having BCB as taught by Kim to prevent errors in the TFT operation by parasitic capacitance.

6. Claims 17-21, 23, 24, 29, 30 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki '233, in view of Yamazaki (JP. Patent No. 06-296,023) of record.

With respect to claim 17, Yamazaki '233 teaches a semiconductor device substantially as claimed including:

a substrate (11);

a first insulating film (32a) provided over the substrate (11);

a second insulating film (32b) provided over the first insulating film (32a);

a semiconductor film (33) provided over the second insulating film (32b);

a channel region (28) provided in the semiconductor film (33); and

a gate electrode (40) provided over the channel region (28) with a gate insulating film (35) therebetween,

wherein an impurity concentration in an interface between said first insulating film (32a) and the second insulating film (32b) is (E19-E21 atom-cm^{-3}) higher than an impurity concentration in an interface between the second insulating film (32b) and the channel region (28) (E11 atom-cm^{-3}). (See Fig. 11A).

Thus, Yamazaki '233 is shown to teach all the features of the claim with the exception of explicitly disclosing the thickness of the first and second insulating film.

However, Yamazaki '023 teaches form the first (302) and second (303) insulating film over the substrate such that the second insulating film (303) is thinner than the first insulating film (302) to prevent contaminant out diffusion from the substrate. (See Fig. 3, [0036-0037]).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the second insulating film of Yamazaki '233 to be thinner than the first insulating film as taught by Yamazaki '023 to prevent contaminant out diffusion from the substrate.

With respect to claim 18, semiconductor device of Yamazaki '233 is capable of incorporated into one selected from the group consisting of a personal computer, a video camera, a mobile computer, a goggle type display, a player using a recording medium, a digital camera, a cellular phone, and an electronic book, as claimed.

With respect to claim 19, the semiconductor film (33) of Yamazaki '233 comprises a material selected from the group consisting of silicon and Si_xGe_{1-x}.

With respect to claim 20, the semiconductor film (33) of Yamazaki '233 comprises crystalline semiconductor.

With respect to claim 21, the substrate (11) of Yamazaki '233 is selected from the group consisting of an insulating substrate.

With respect to claim 23, the second insulating film (32b) of Yamazaki '233 comprises a material selected from the group consisting of silicon oxide.

With respect to claim 24, the first insulating film (32a) of Yamazaki '233 comprises a material selected from the group consisting of silicon oxide.

With respect to claims 29 and 30, the first (302) and second (303) insulating film of Yamazaki '023 have a thickness of (200-500 nm and 100-200 nm, respectively), thus, met the claimed range.

Note that, the claimed thicknesses, 100-500 nm and 10-100 nm, do not appear to be critical in insulating the substrate or the functionality of the device as a whole.

Note that the specification contains no disclosure of either the *critical nature of the claimed thickness of the first (100-500 nm) and second (10-100 nm) insulating film* of any unexpected results arising therefrom. Where patentability is aid to based upon particular chosen dimension or upon another variable recited in a claim, the Applicant must show that the chosen dimension are critical. *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

With respect to claim 33, since the first insulating film was exposed to oxygen in the doping step, thus, the impurity of Yamazaki comprises oxygen.

7. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki '233 and Yamazaki '023 as applied to claim 17 above, and further in view of Kim '954.

Yamazaki teaches the semiconductor device as described in claim 17 above including a gate insulating film (35) formed between the gate electrode (40) and the channel region (28).

Thus, Yamazaki is shown to teach all the features of the claim with the exception of utilizing organic resin for the gate insulating film.

However, Kim teaches a semiconductor device having a gate insulating film (157) comprising an organic resin (BCB) is formed between a gate electrode (113) and channel region (119). (See Fig. 13D).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the gate insulating film of Yamazaki utilizing organic resin having BCB as taught by Kim to prevent errors in the TFT operation by parasitic capacitance.

8. Claims 25-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki '233 as applied to claims 1 and 17 above, and further in view of Yamazaki '023.

Yamazaki '233 teaches a semiconductor device having a first insulating film (32a) provided over substrate (11) and a second insulating film (32b) provided over the first insulating film (32a).

Thus, Yamazaki '233 is shown to teach all the features of the claim with the exception of explicitly disclosing the thicknesses of the first and second insulating film.

Note that, the claimed thicknesses, 100-500 nm and 10-100 nm, do not appear to be critical in insulating the substrate or the functionality of the device as a whole.

However, Yamazaki '023 teaches the first (302) and second (303) insulating film are provided over the substrate (301) having a thickness of 200-500 nm and 100-200 nm, respectively, thus, met the claimed range to prevent contaminant out diffusion from the substrate. (See Fig. 3, [0036-0037]).

Note that the specification contains no disclosure of either the *critical nature of the claimed thickness of the first (100-500 nm) and second (10-100 nm) insulating film* of any unexpected results arising therefrom. Where patentability is aid to based upon particular chosen dimension or upon another variable recited in a claim, the Applicant must show that the chosen dimension are critical. *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the first and second insulating films of Yamazaki '233 to have the thicknesses as taught by Yamazaki '023 to prevent contaminant out diffusion from the substrate.

Response to Arguments

9. Applicant's arguments filed October 19, 2005 have been fully considered but they are not persuasive.

Regarding the response to the argument of the previous Office Action, Applicant appears to contend that since the same reference were used to rejected the amended claims, the arguments are not moot.

However, the claim once amended, add or remove limitation, the scope of the claim has changed, thus argument regarding the new scope is moot.

Moreover, the rejection have been changed from obviousness to anticipation, because the new scope of the amendment. Thus argument regarding the new scope is moot.

Regarding the impurity concentration, Applicant argues that patent '233 fails to teach or suggest the claimed feature of an impurity concentration in an interface between the first insulating film and the second insulating film that is higher than an impurity concentration in an interface between the second insulating film and the channel region, as set forth in claims 1, 7, and 17.

Applicant should have reviewed the teaching as shown in Fig. 11A. Patent '233 teaches that the first insulating film (32A) is exposed, thus, doped with phosphorous or a halogen in addition to oxygen, while the second insulating film (32B) is undoped. Therefore, one having ordinary skill in the art should have concluded that, the interface between the first and second insulating film have higher impurity (phosphorous, halogen or oxygen) concentration than that of the interface between the second insulating film (32B) and the channel region (28).

Note that, the first insulating film of the instant application only needs to be exposed to the atmosphere, the impurity has already accumulated.

Applicant argues something about *interface state density.* Since neither the claims nor the rejection mention anything about the *interface density state,* the argument is moot.

The disclosure can be found in Fig. 11A and page 11 of patent '233.

For the future prosecution, Applicant is reminded that the support for new limitation, as that of new claims 31-33, should be point out in the Remarks. That will help shorten the time to look for the support, specially in a jumbo case such as this application.

Conclusion

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh D. Mai whose telephone number is (571) 272-1710. The examiner can normally be reached on 8:00AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ANH D. MAI
PRIMARY EXAMINER